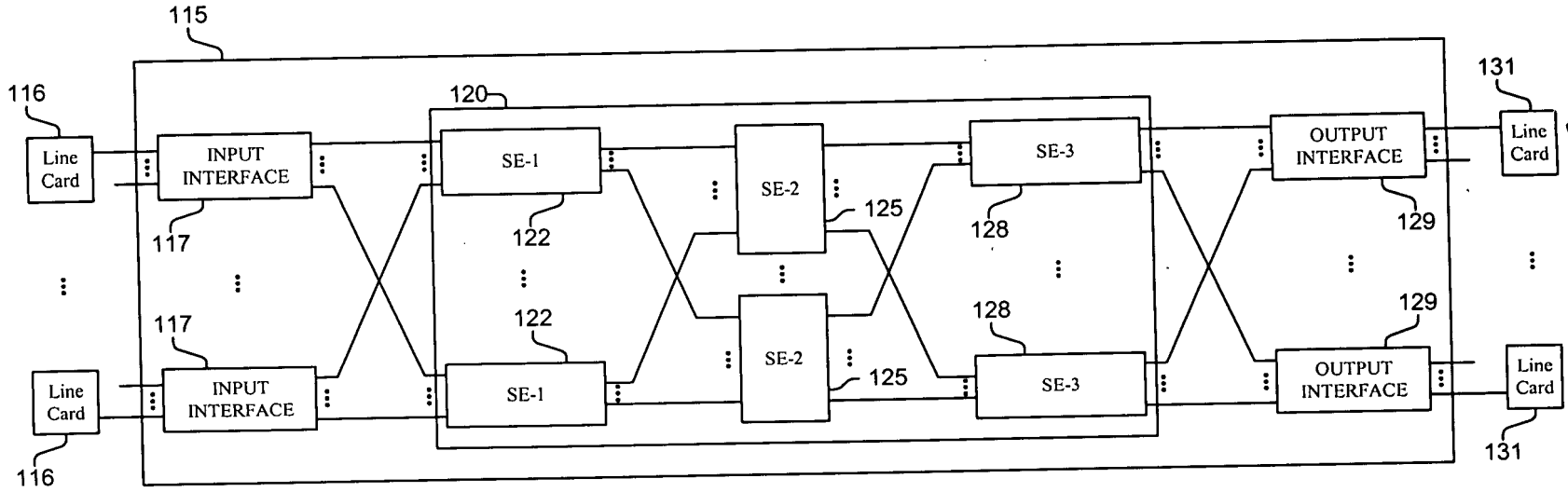

FIG. 1A

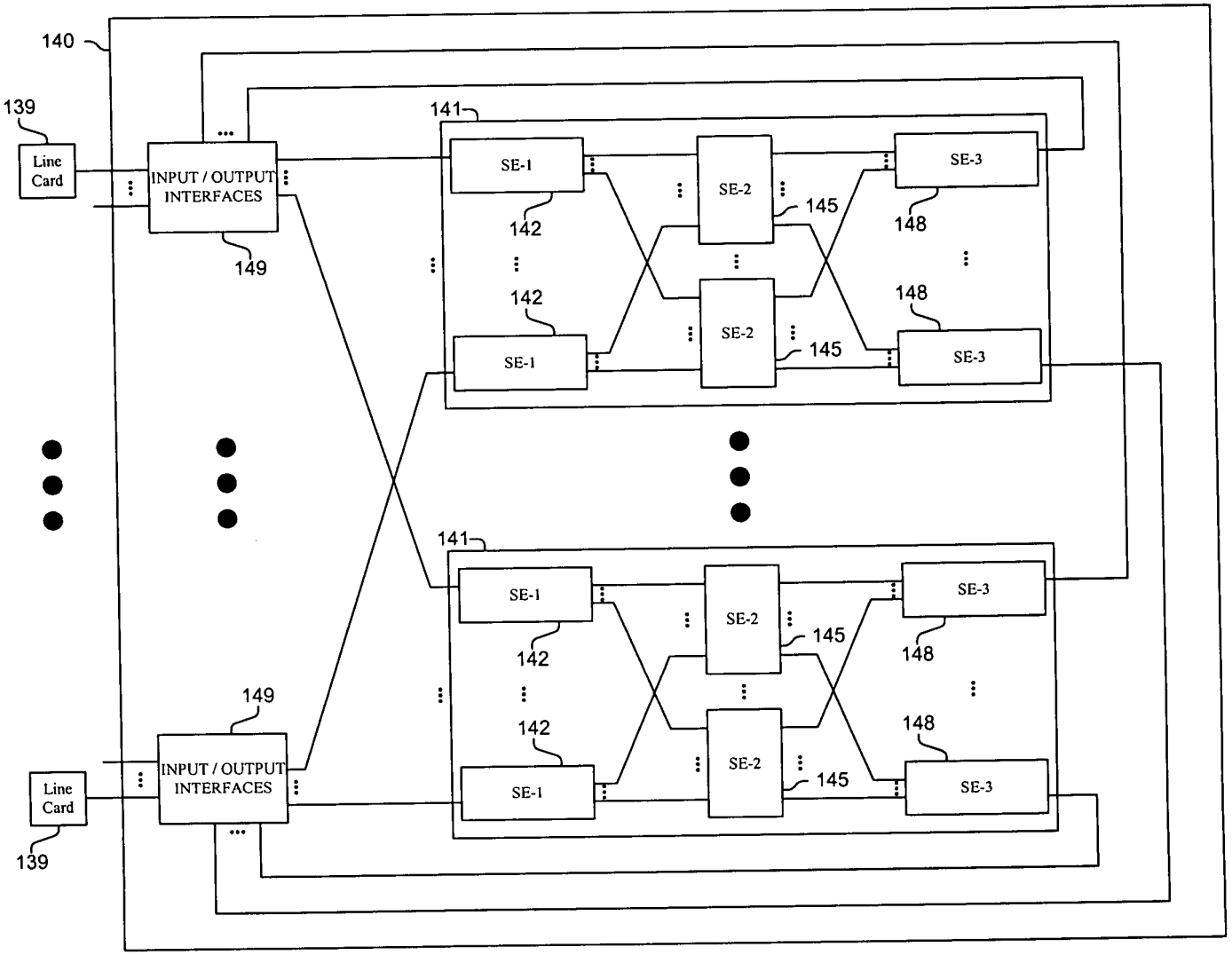

FIG. 1B

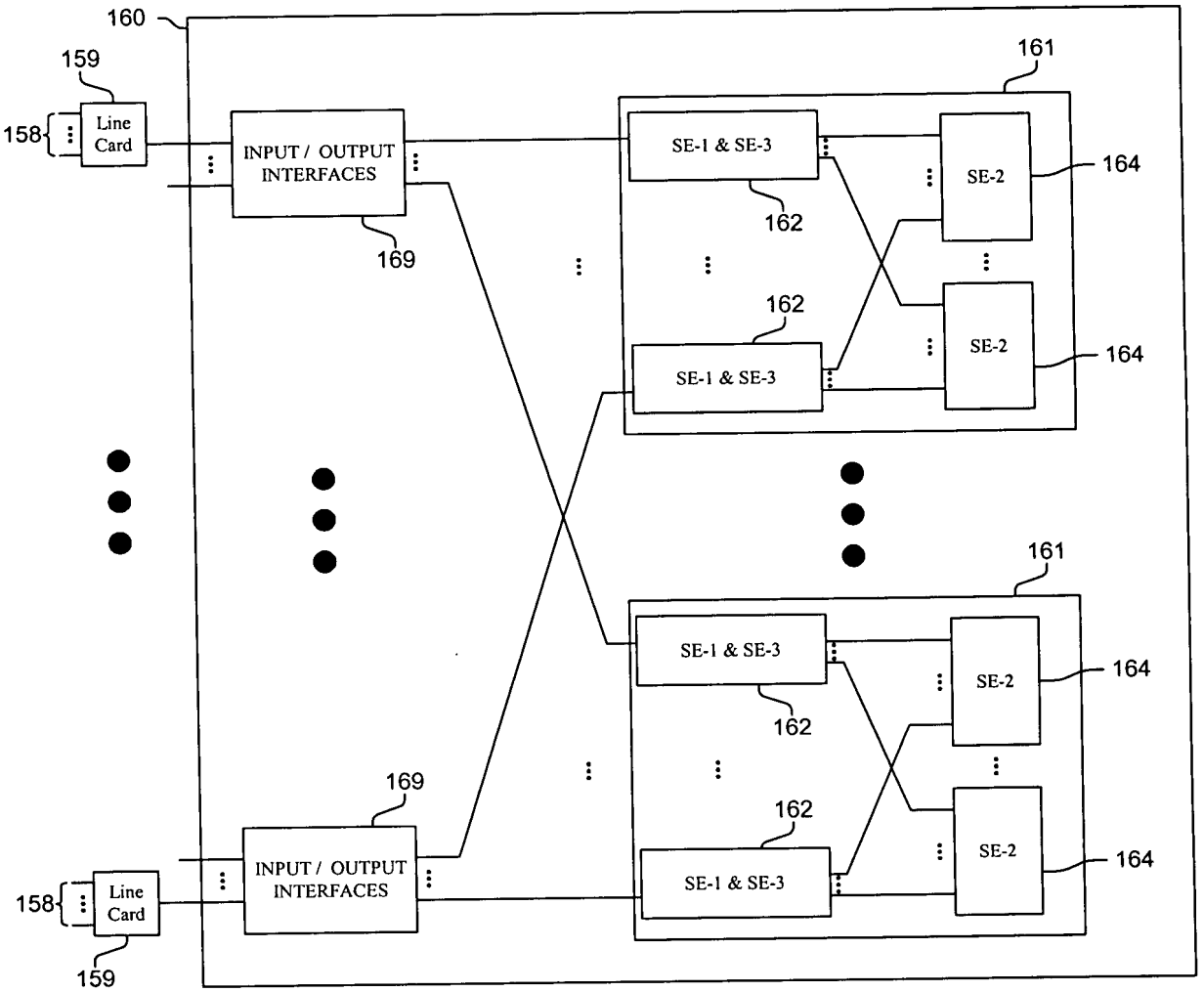
160
159
158
Line Card
INPUT / OUTPUT INTERFACES
169
161
SE-1 & SE-3
162
SE-2
164
Line Card
159

FIG. 1C

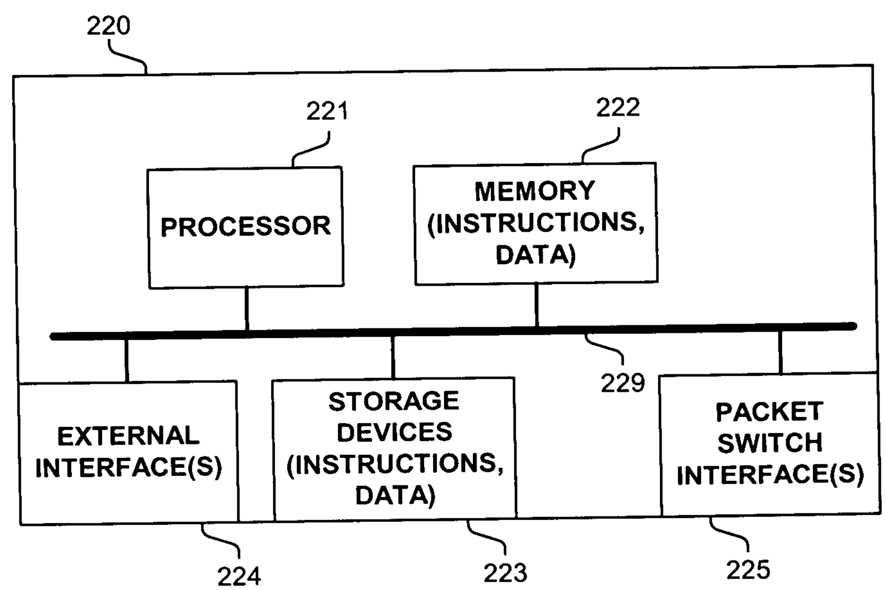
220
221
222
PROCESSOR
MEMORY (INSTRUCTIONS, DATA)
229
EXTERNAL INTERFACE(S)
STORAGE DEVICES (INSTRUCTIONS, DATA)
PACKET SWITCH INTERFACE(S)
224
223
225

FIG. 2A

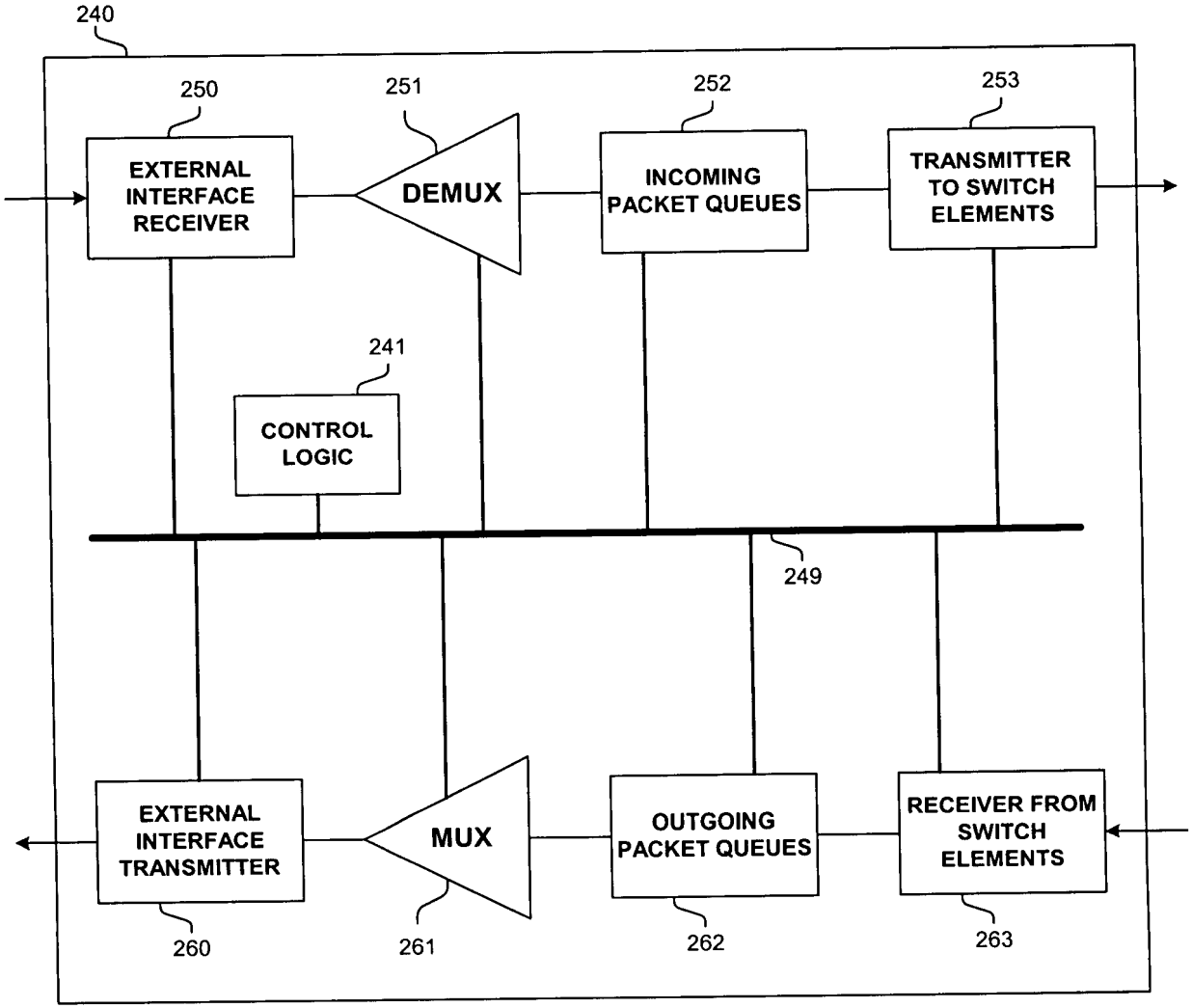

FIG. 2B

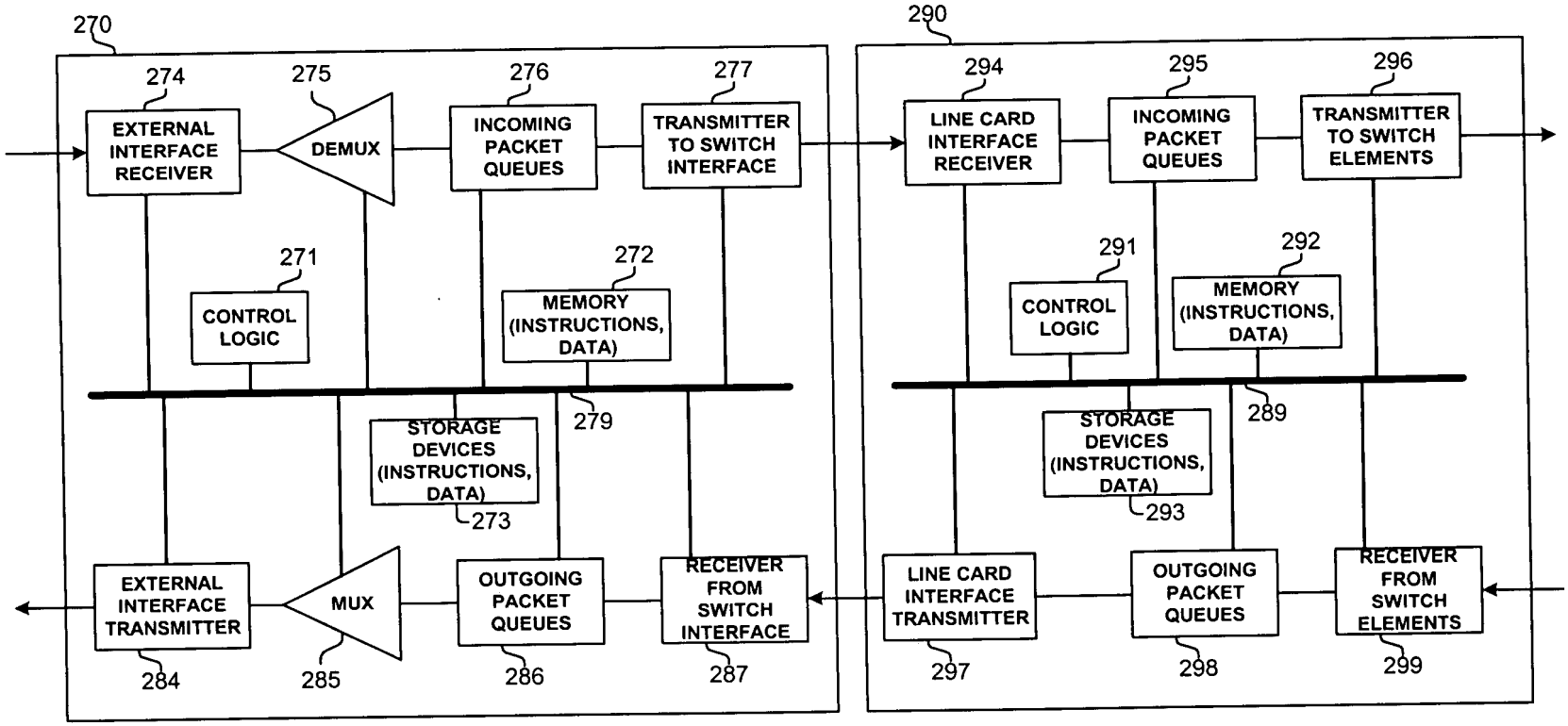

FIG. 2C

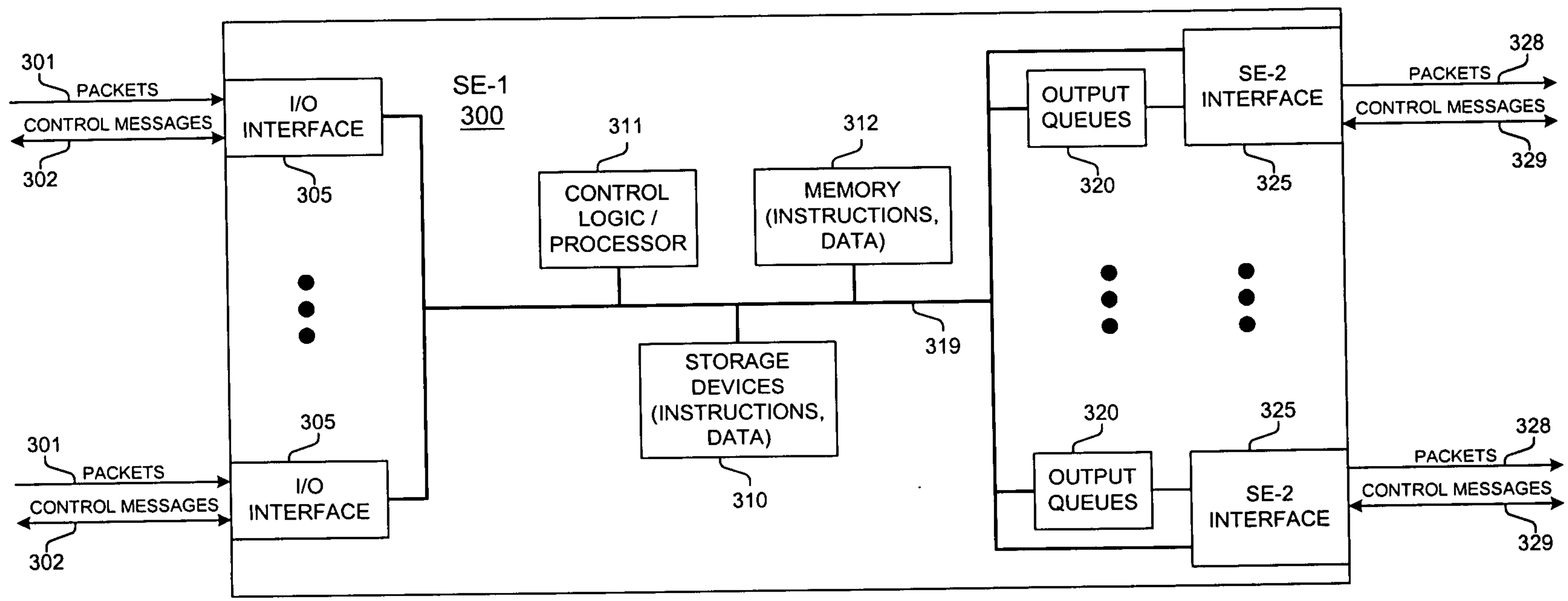
301
PACKETS
CONTROL MESSAGES
302
I/O
INTERFACE
305
SE-1
300
311
CONTROL
LOGIC /
PROCESSOR
312
MEMORY
(INSTRUCTIONS,
DATA)
STORAGE
DEVICES
(INSTRUCTIONS,
DATA)
310
319
OUTPUT
QUEUES
320
SE-2
INTERFACE
325
328
PACKETS
CONTROL MESSAGES
329

FIG. 3A

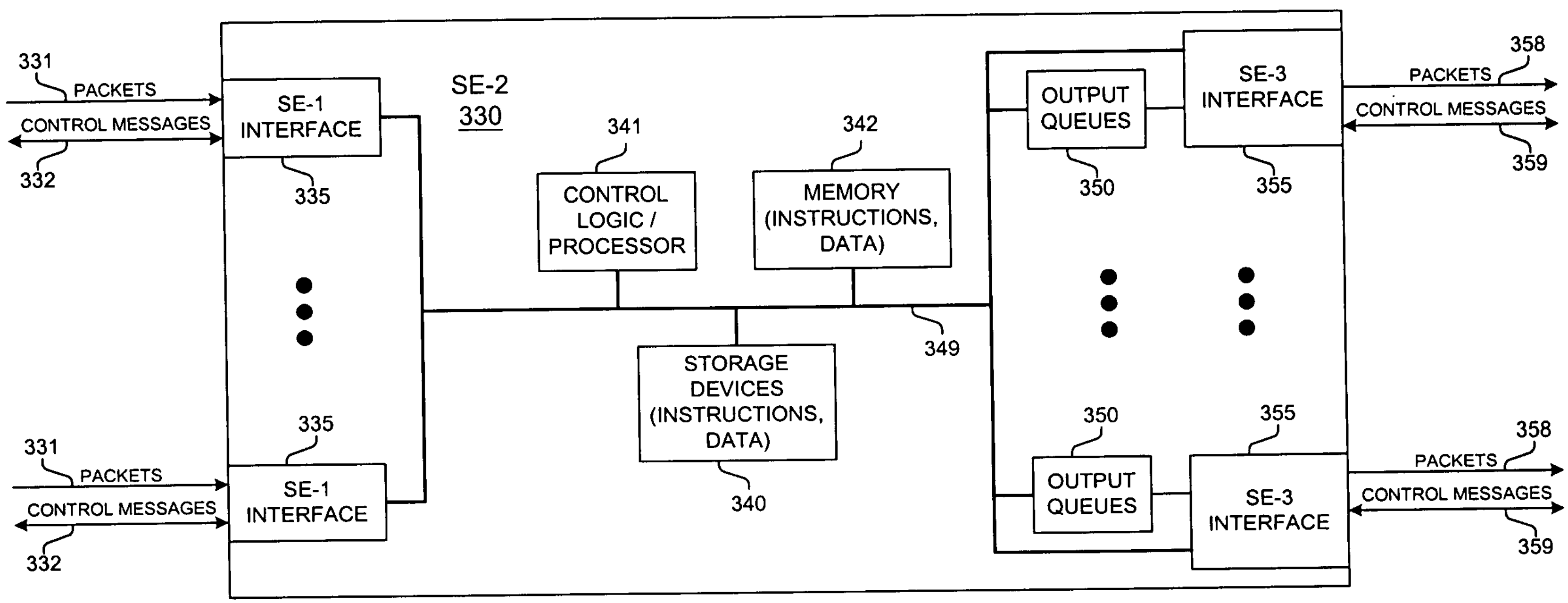
331
PACKETS
CONTROL MESSAGES
332
SE-1
INTERFACE
335
SE-2
330
341
CONTROL
LOGIC /
PROCESSOR
342
MEMORY
(INSTRUCTIONS,
DATA)
STORAGE
DEVICES
(INSTRUCTIONS,
DATA)
340
349
OUTPUT
QUEUES
350
SE-3
INTERFACE
355
358
PACKETS
CONTROL MESSAGES
359

FIG. 3B

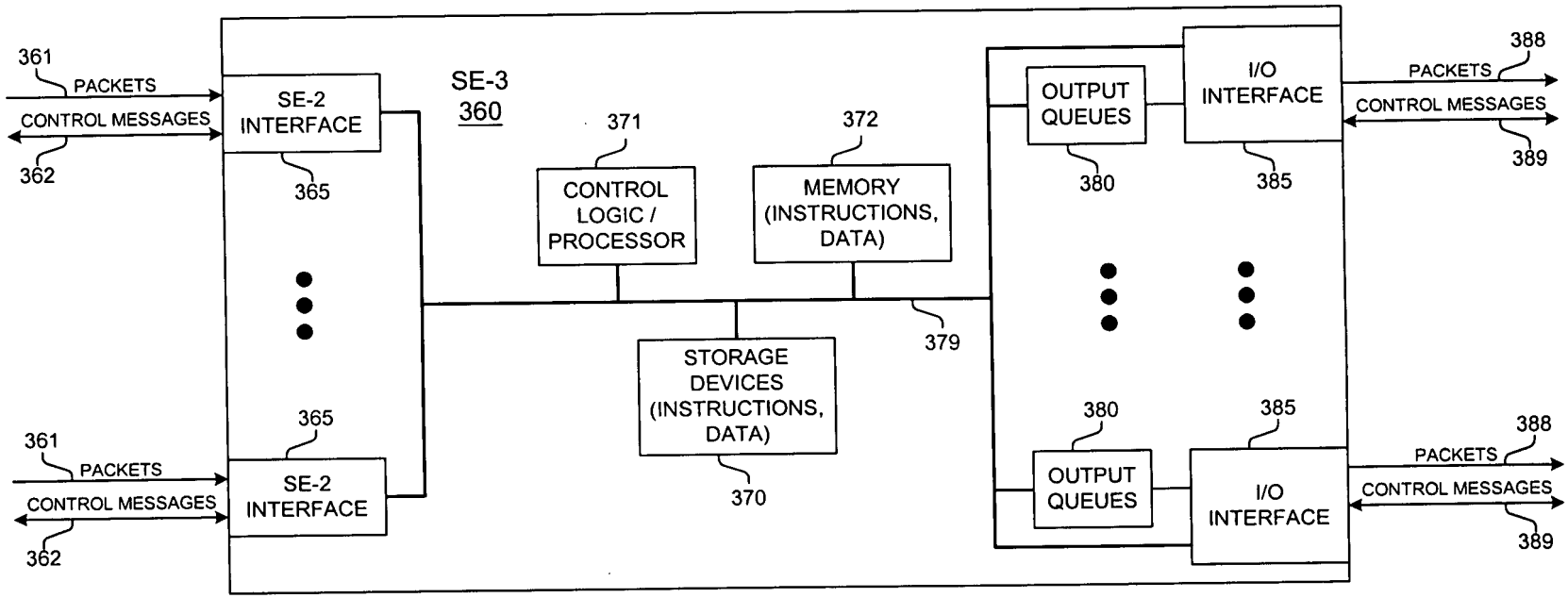
361
PACKETS
CONTROL MESSAGES
362
SE-2 INTERFACE
365
SE-3
360
371
CONTROL LOGIC / PROCESSOR
372
MEMORY (INSTRUCTIONS, DATA)
379
STORAGE DEVICES (INSTRUCTIONS, DATA)
370
OUTPUT QUEUES
380
I/O INTERFACE
385
388
PACKETS
CONTROL MESSAGES
389

FIG. 3C

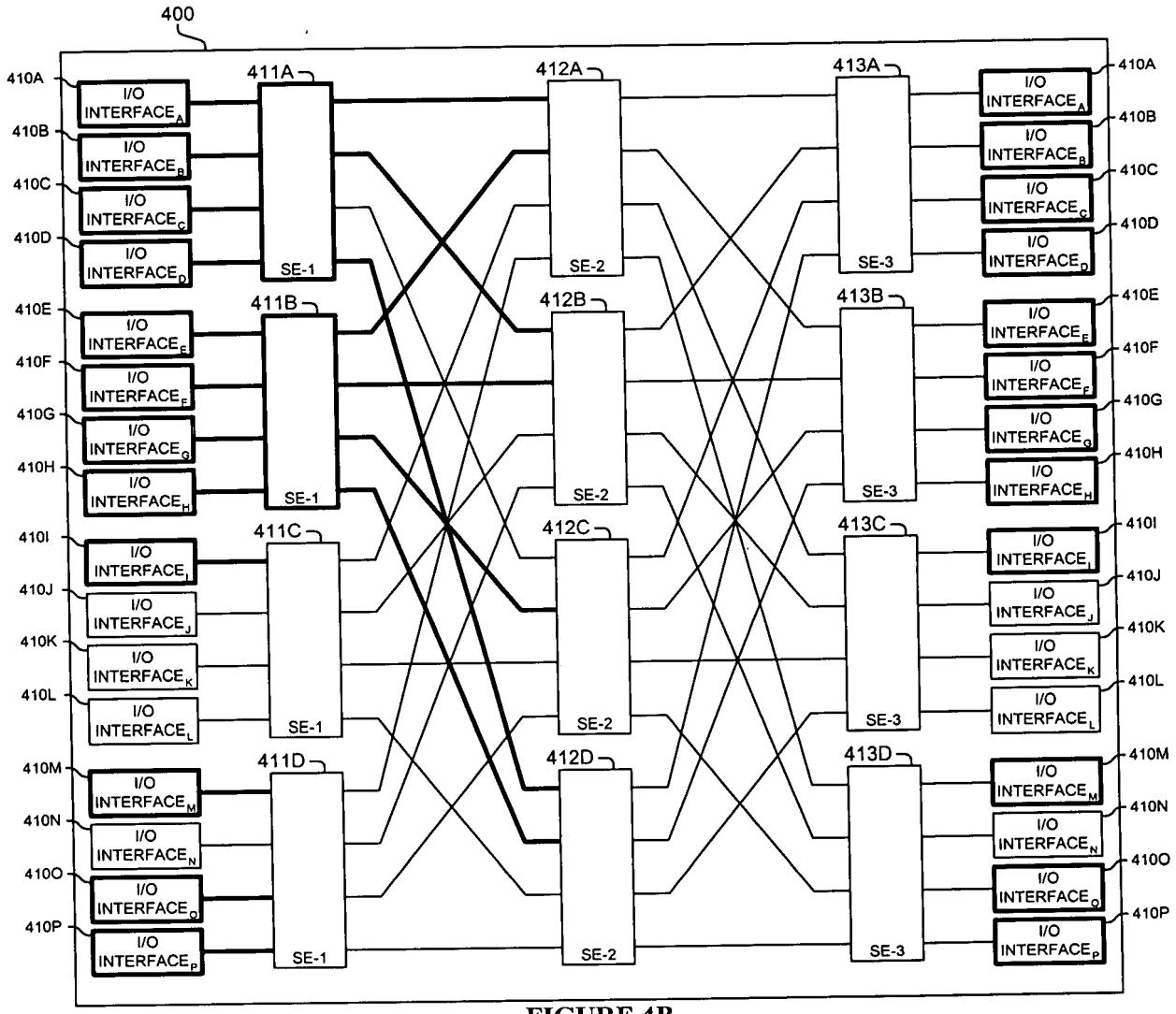
400
410A
410B
410C
410D
410E
410F
410G
410H
410I
410J
410K
410L
410M
410N
410O
410P
I/O INTERFACE$_A$
I/O INTERFACE$_B$
I/O INTERFACE$_C$
I/O INTERFACE$_D$
I/O INTERFACE$_E$
I/O INTERFACE$_F$
I/O INTERFACE$_G$
I/O INTERFACE$_H$
I/O INTERFACE$_I$
I/O INTERFACE$_J$
I/O INTERFACE$_K$
I/O INTERFACE$_L$
I/O INTERFACE$_M$
I/O INTERFACE$_N$
I/O INTERFACE$_O$
I/O INTERFACE$_P$
411A
411B
411C
411D
412A
412B
412C
412D
413A
413B
413C
413D
SE-1
SE-2
SE-3

FIGURE 4B

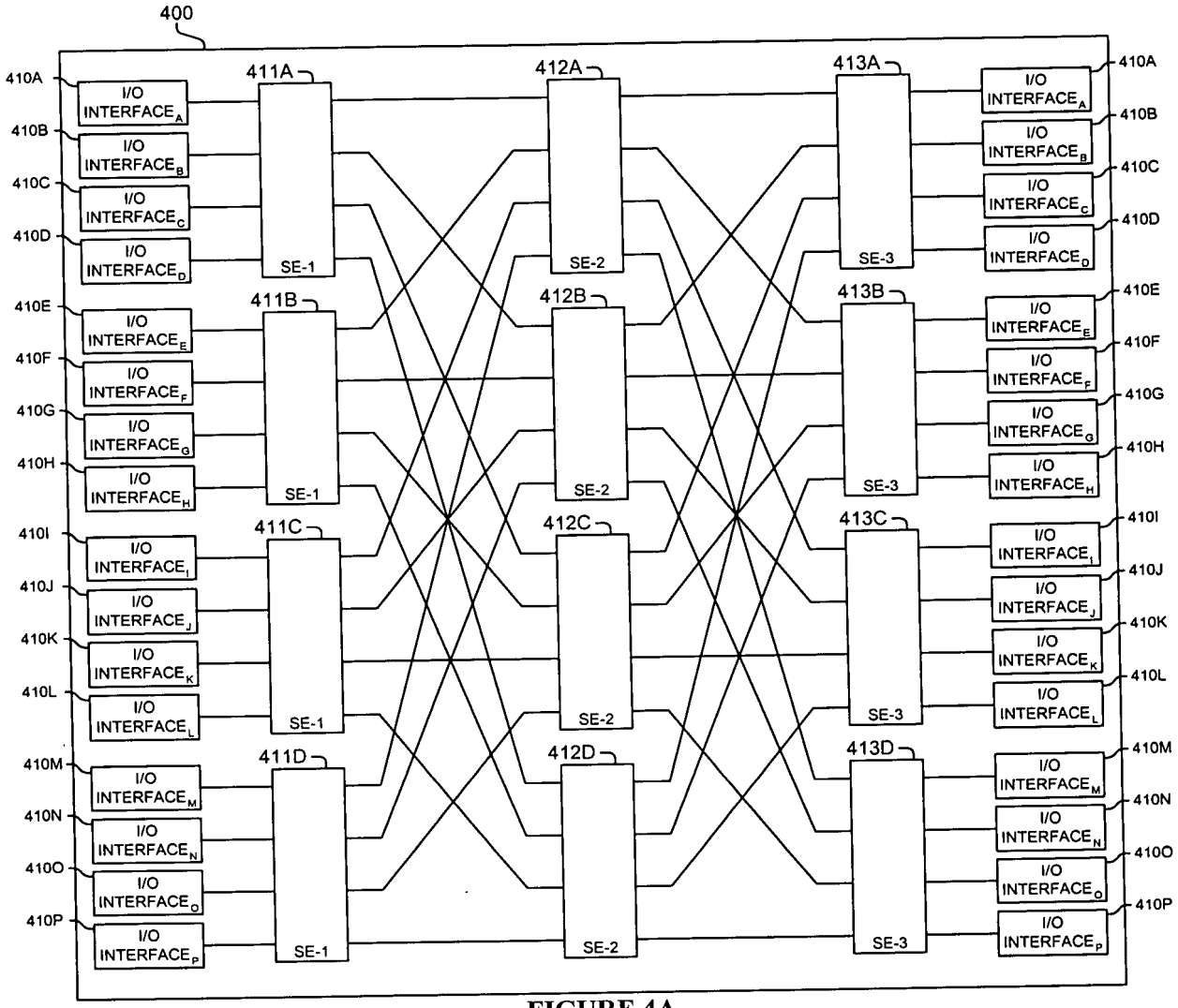
400
410A
410B
410C
410D
410E
410F
410G
410H
410I
410J
410K
410L
410M
410N
410O
410P
I/O INTERFACE$_A$
I/O INTERFACE$_B$
I/O INTERFACE$_C$
I/O INTERFACE$_D$
I/O INTERFACE$_E$
I/O INTERFACE$_F$
I/O INTERFACE$_G$
I/O INTERFACE$_H$
I/O INTERFACE$_I$
I/O INTERFACE$_J$
I/O INTERFACE$_K$
I/O INTERFACE$_L$
I/O INTERFACE$_M$
I/O INTERFACE$_N$
I/O INTERFACE$_O$
I/O INTERFACE$_P$
411A
411B
411C
411D
412A
412B
412C
412D
413A
413B
413C
413D
SE-1
SE-2
SE-3

FIGURE 4A

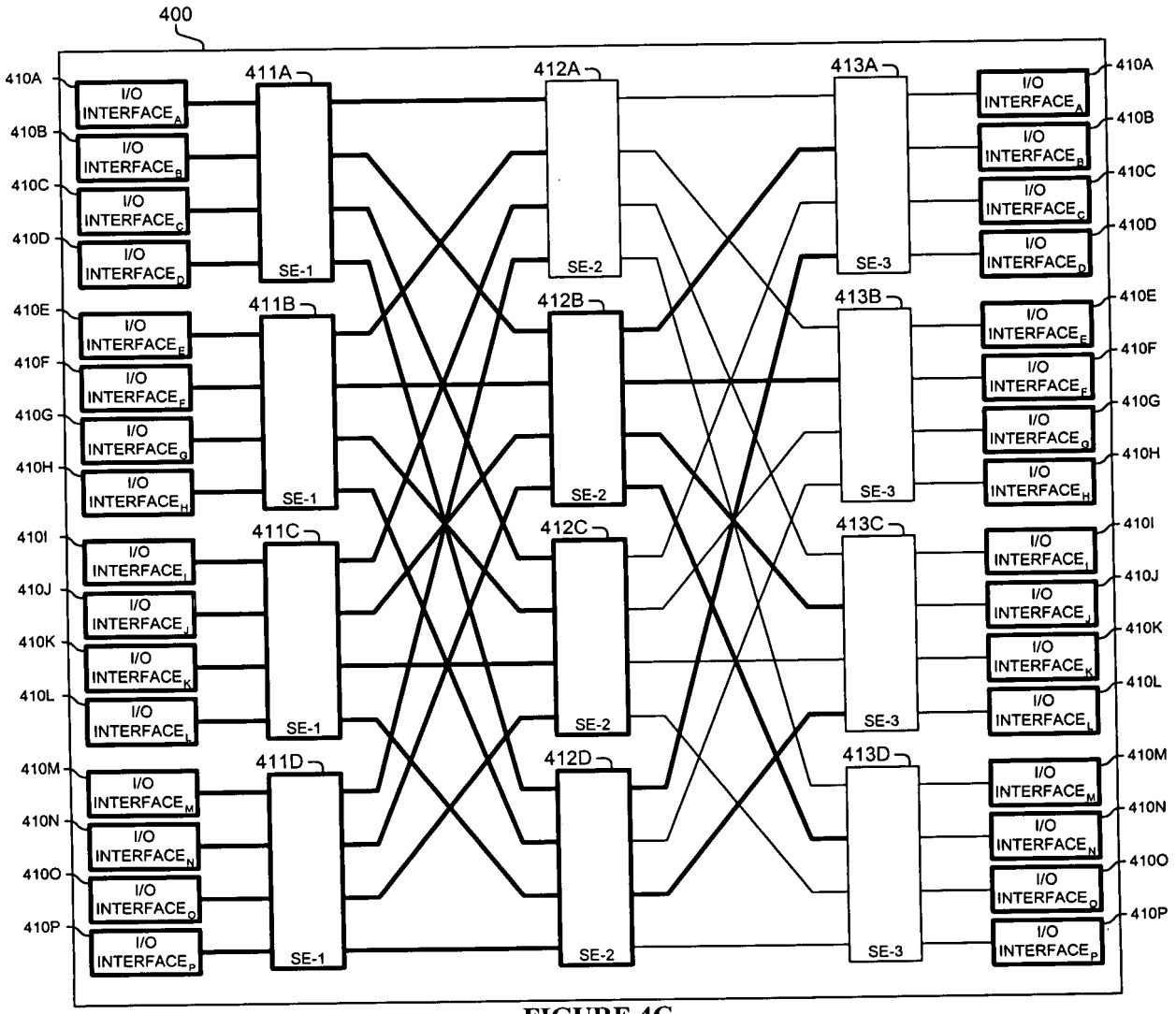

FIGURE 4C

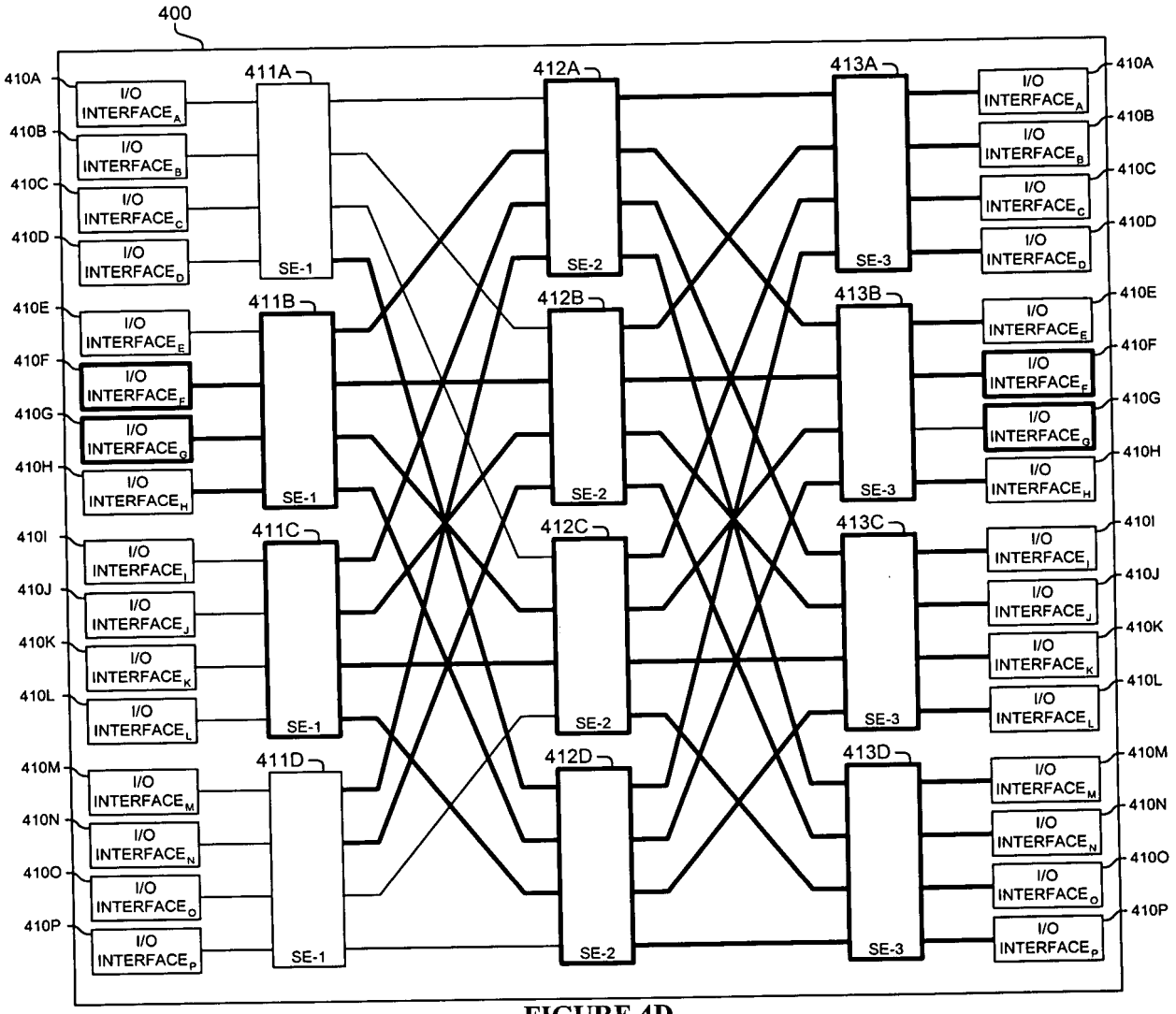

FIGURE 4D

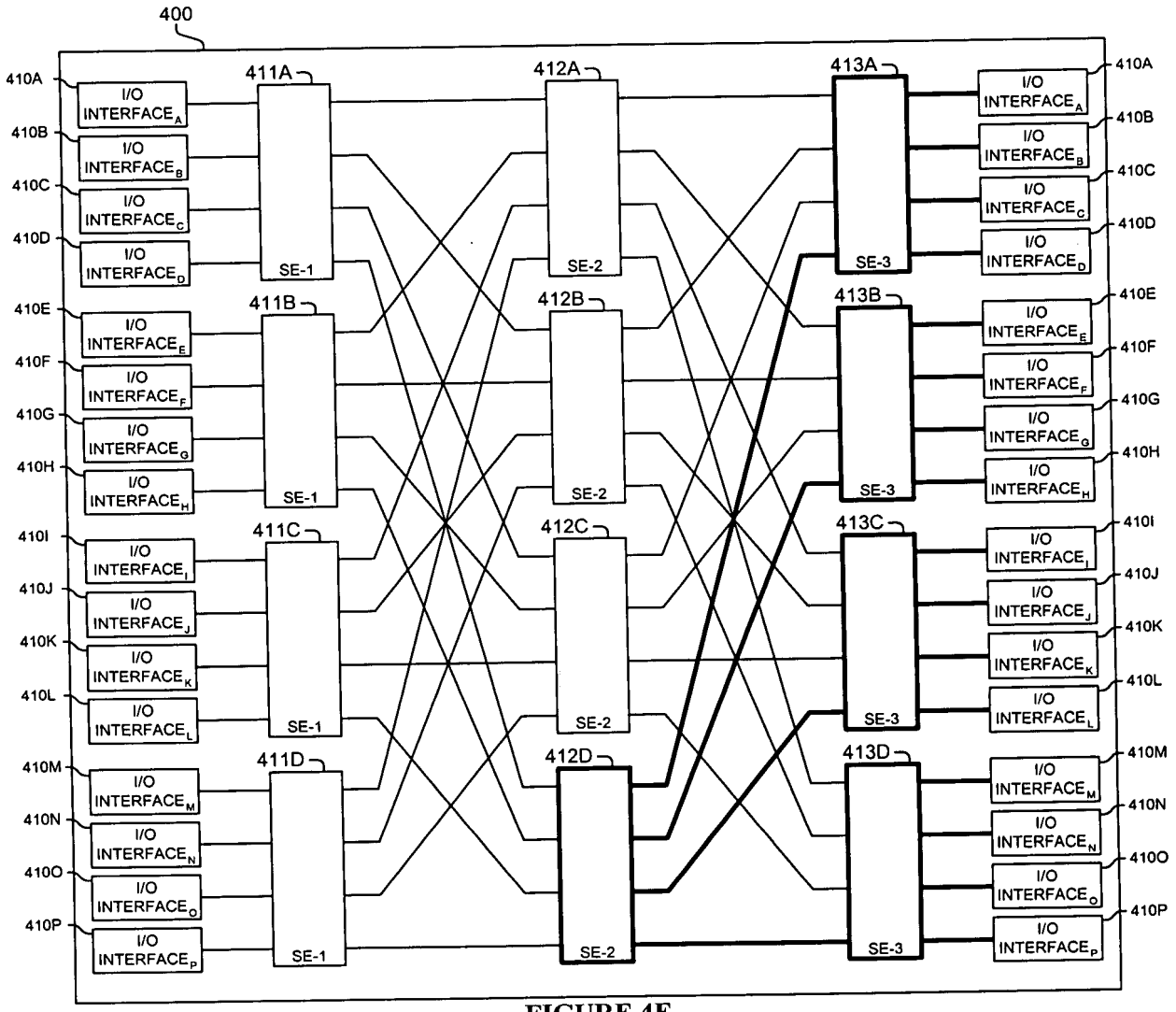

FIGURE 4E

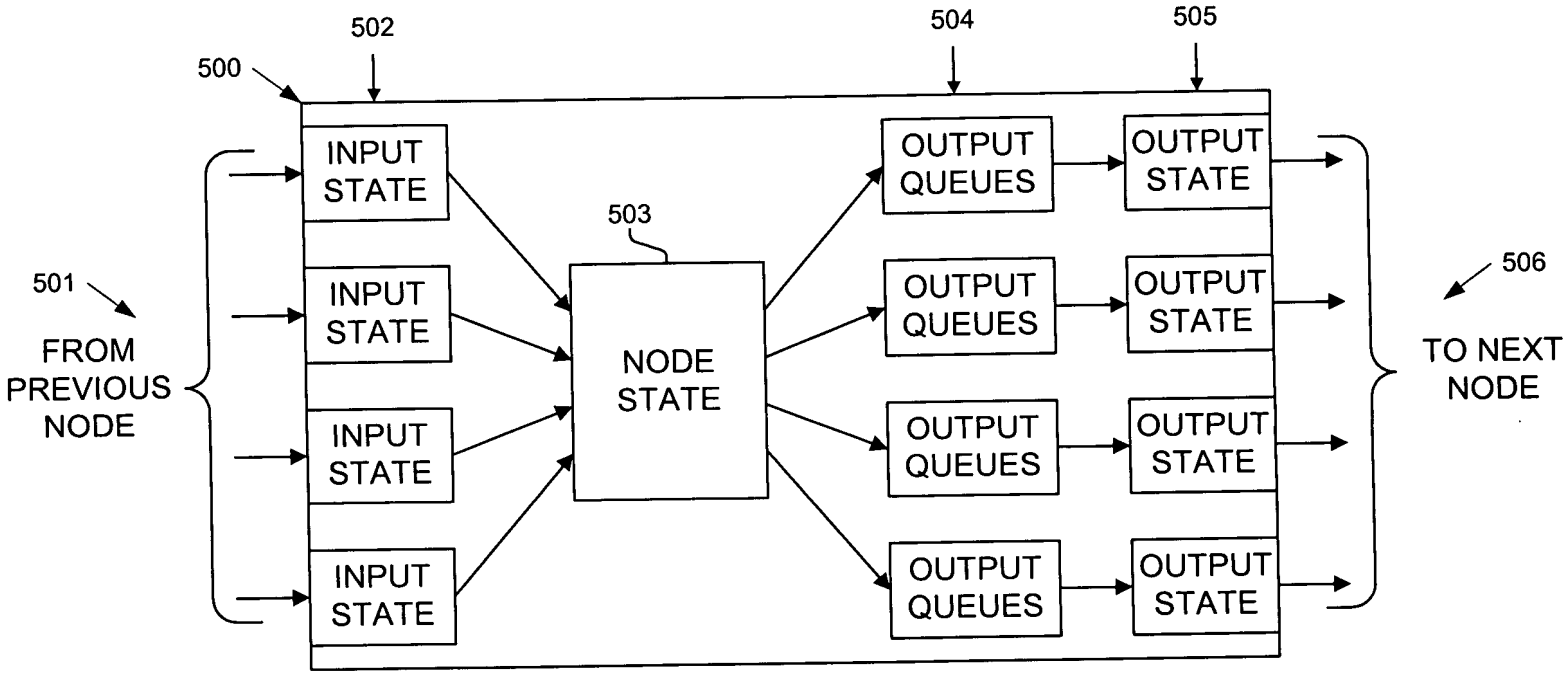

FIGURE 5A

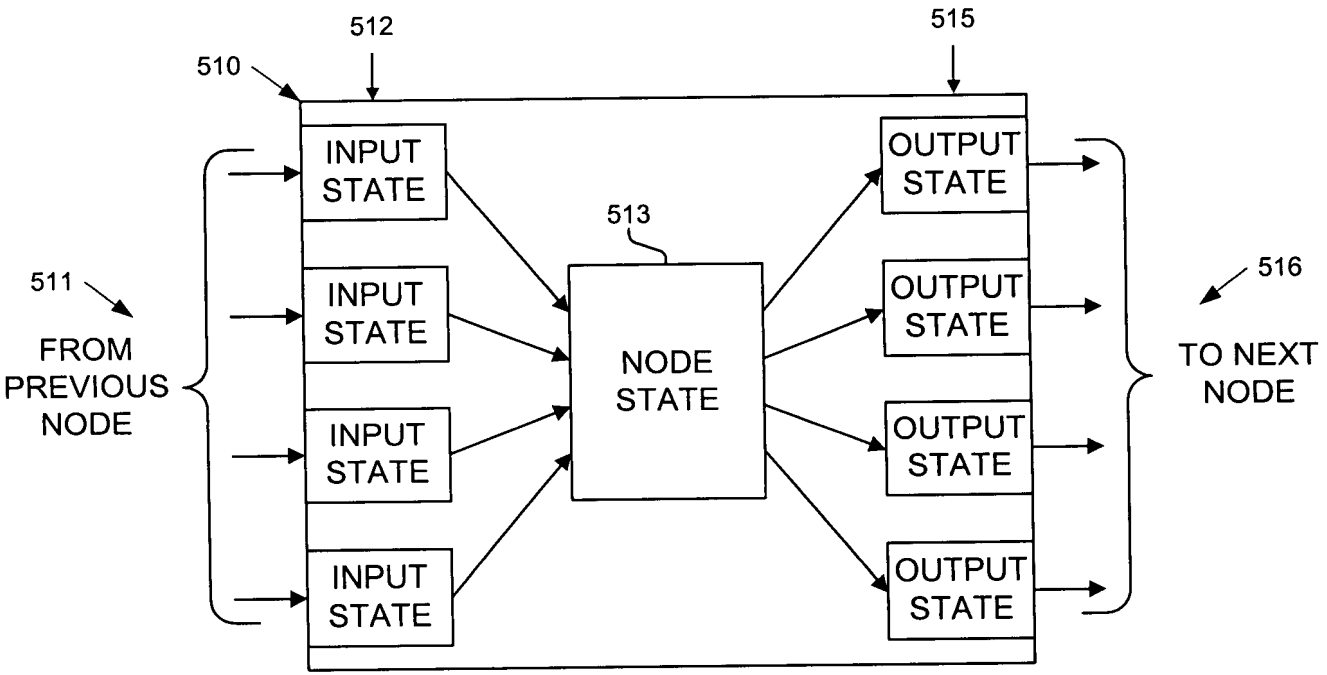

FIGURE 5B

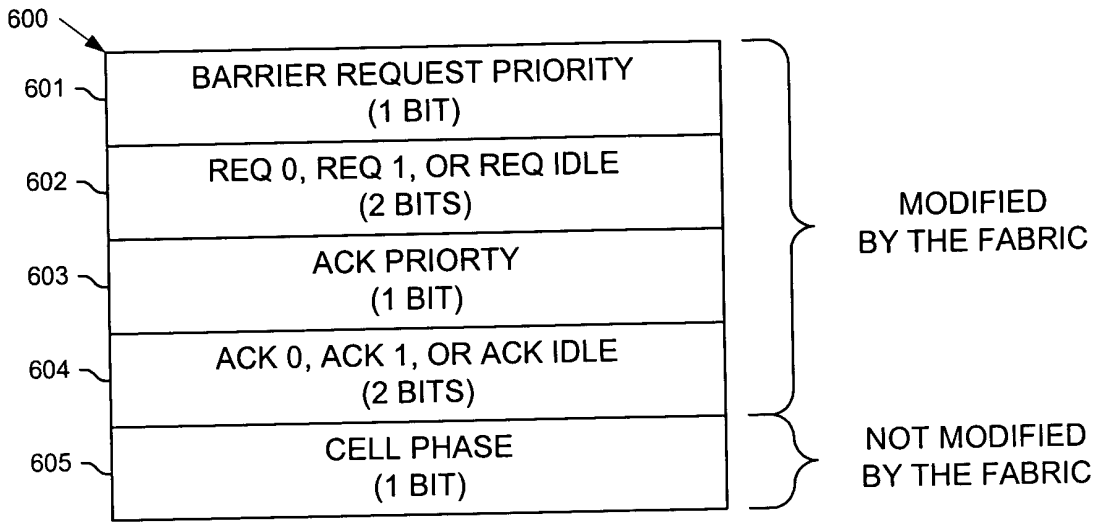
600
601
BARRIER REQUEST PRIORITY
(1 BIT)
602
REQ 0, REQ 1, OR REQ IDLE
(2 BITS)
603
ACK PRIORTY
(1 BIT)
604
ACK 0, ACK 1, OR ACK IDLE
(2 BITS)
605
CELL PHASE
(1 BIT)
MODIFIED
BY THE FABRIC
NOT MODIFIED
BY THE FABRIC

FIGURE 6

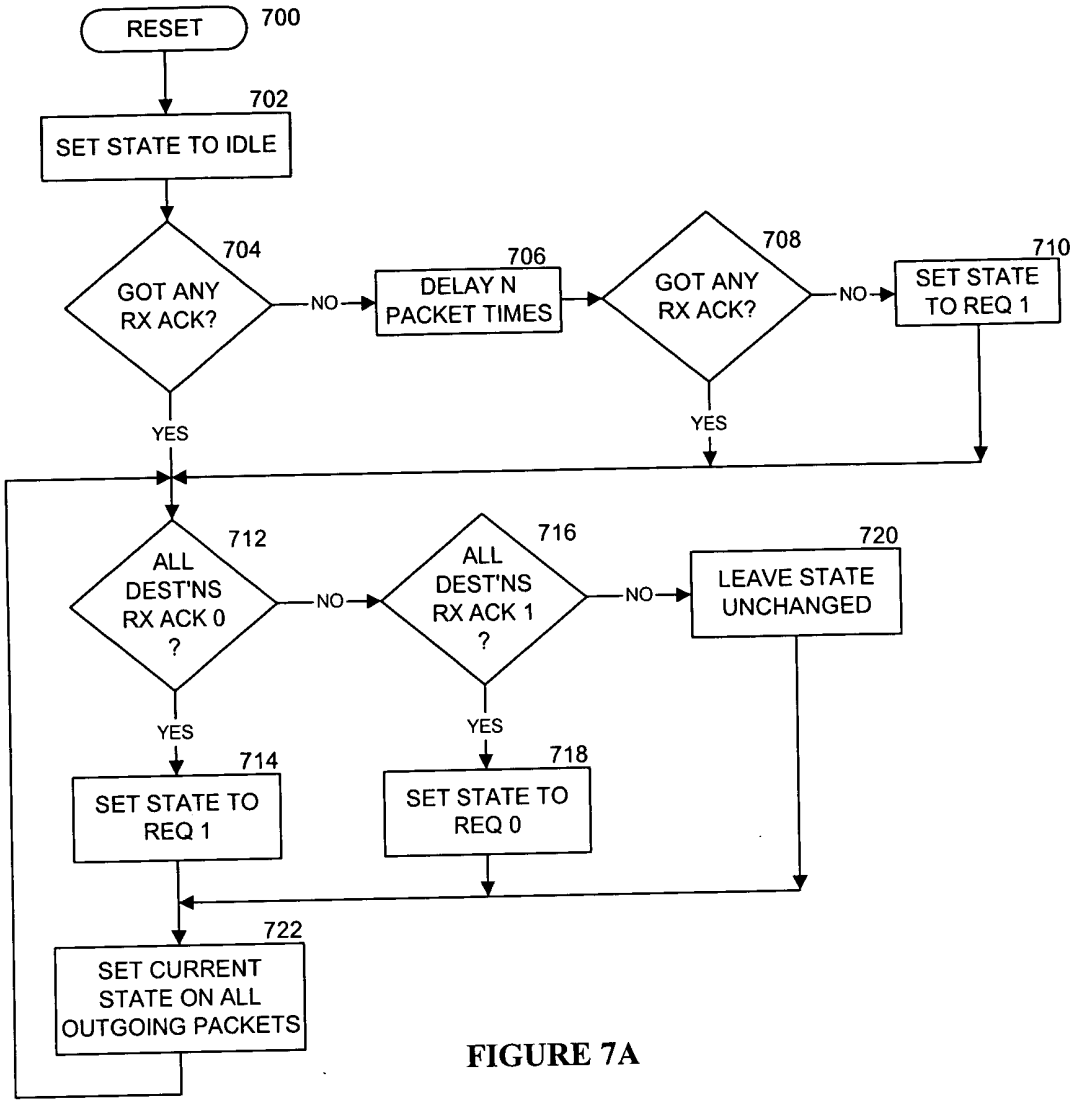
RESET
700
SET STATE TO IDLE
702
GOT ANY RX ACK?
704
NO
DELAY N PACKET TIMES
706
GOT ANY RX ACK?
708
NO
SET STATE TO REQ 1
710
YES
YES
ALL DEST'NS RX ACK 0 ?
712
NO
ALL DEST'NS RX ACK 1 ?
716
NO
LEAVE STATE UNCHANGED
720
YES
YES
SET STATE TO REQ 1
714
SET STATE TO REQ 0
718
SET CURRENT STATE ON ALL OUTGOING PACKETS
722

FIGURE 7A

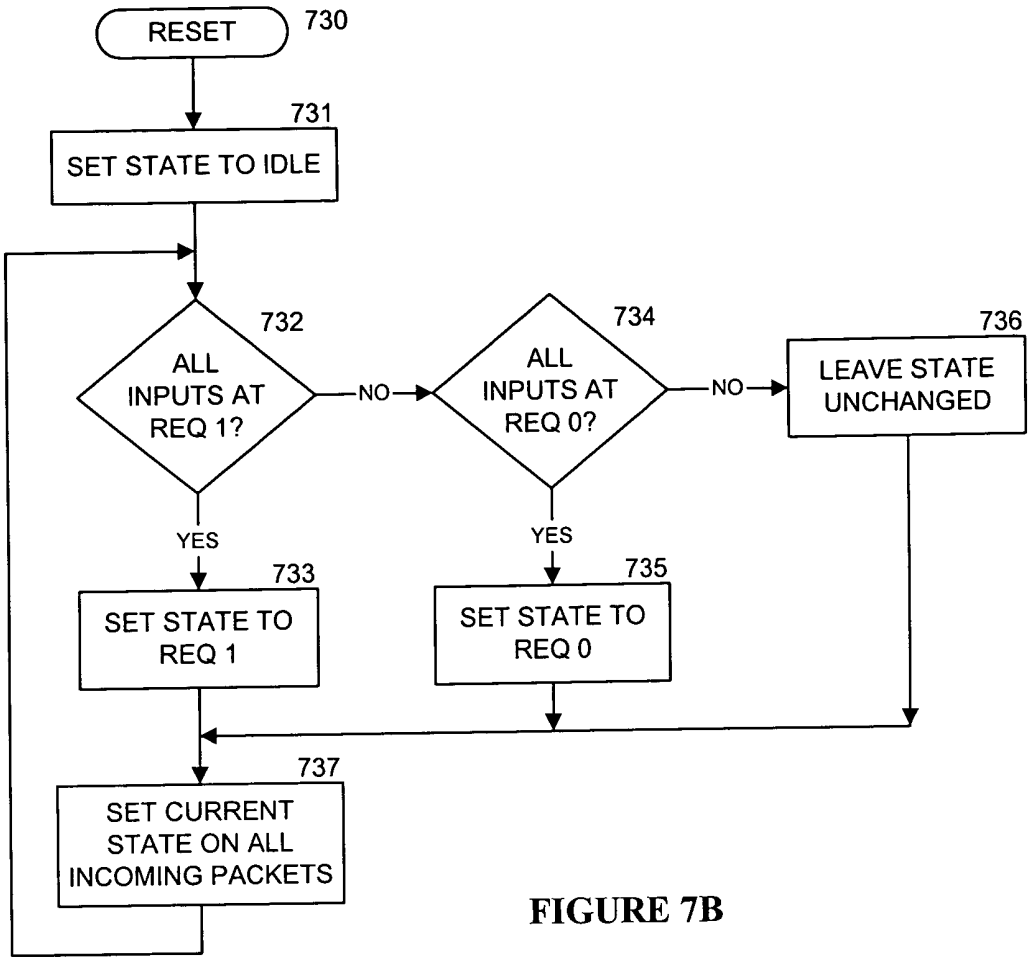
RESET
730
731
SET STATE TO IDLE
732
ALL INPUTS AT REQ 1?
NO
734
ALL INPUTS AT REQ 0?
NO
736
LEAVE STATE UNCHANGED
YES
YES
733
SET STATE TO REQ 1
735
SET STATE TO REQ 0
737
SET CURRENT STATE ON ALL INCOMING PACKETS

FIGURE 7B

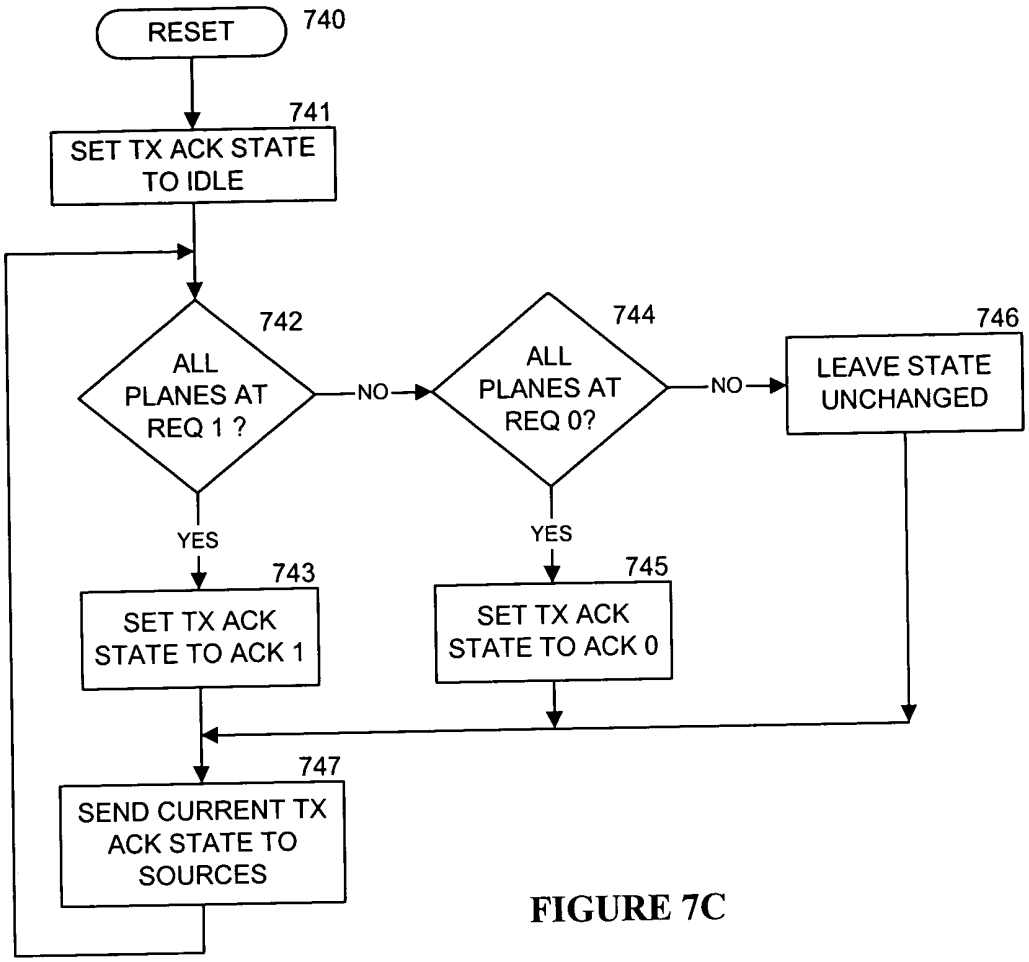
RESET
740
741
SET TX ACK STATE TO IDLE
742
ALL PLANES AT REQ 1 ?
NO
744
ALL PLANES AT REQ 0?
NO
746
LEAVE STATE UNCHANGED
YES
YES
743
SET TX ACK STATE TO ACK 1
745
SET TX ACK STATE TO ACK 0
747
SEND CURRENT TX ACK STATE TO SOURCES

FIGURE 7C

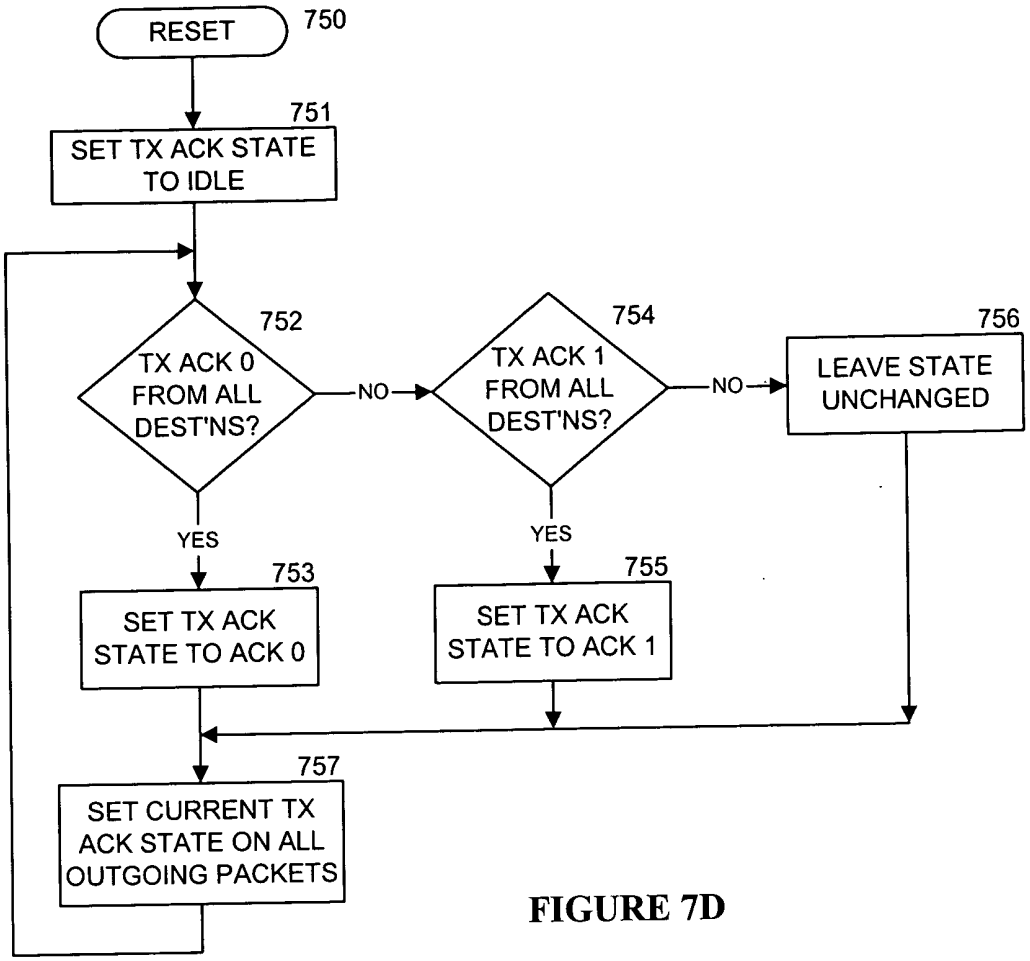
RESET
750
751
SET TX ACK STATE TO IDLE
752
TX ACK 0 FROM ALL DEST'NS?
NO
754
TX ACK 1 FROM ALL DEST'NS?
NO
756
LEAVE STATE UNCHANGED
YES
YES
753
SET TX ACK STATE TO ACK 0
755
SET TX ACK STATE TO ACK 1
757
SET CURRENT TX ACK STATE ON ALL OUTGOING PACKETS

FIGURE 7D

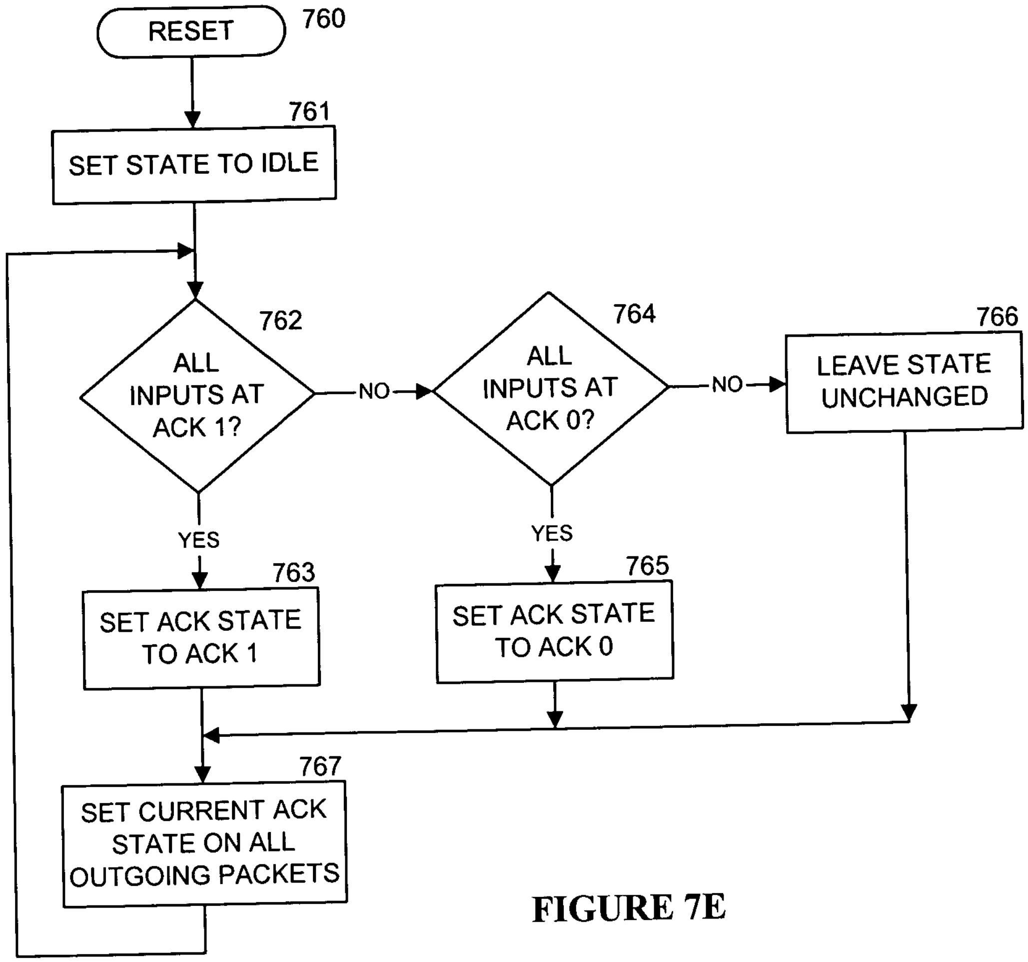

FIGURE 7E

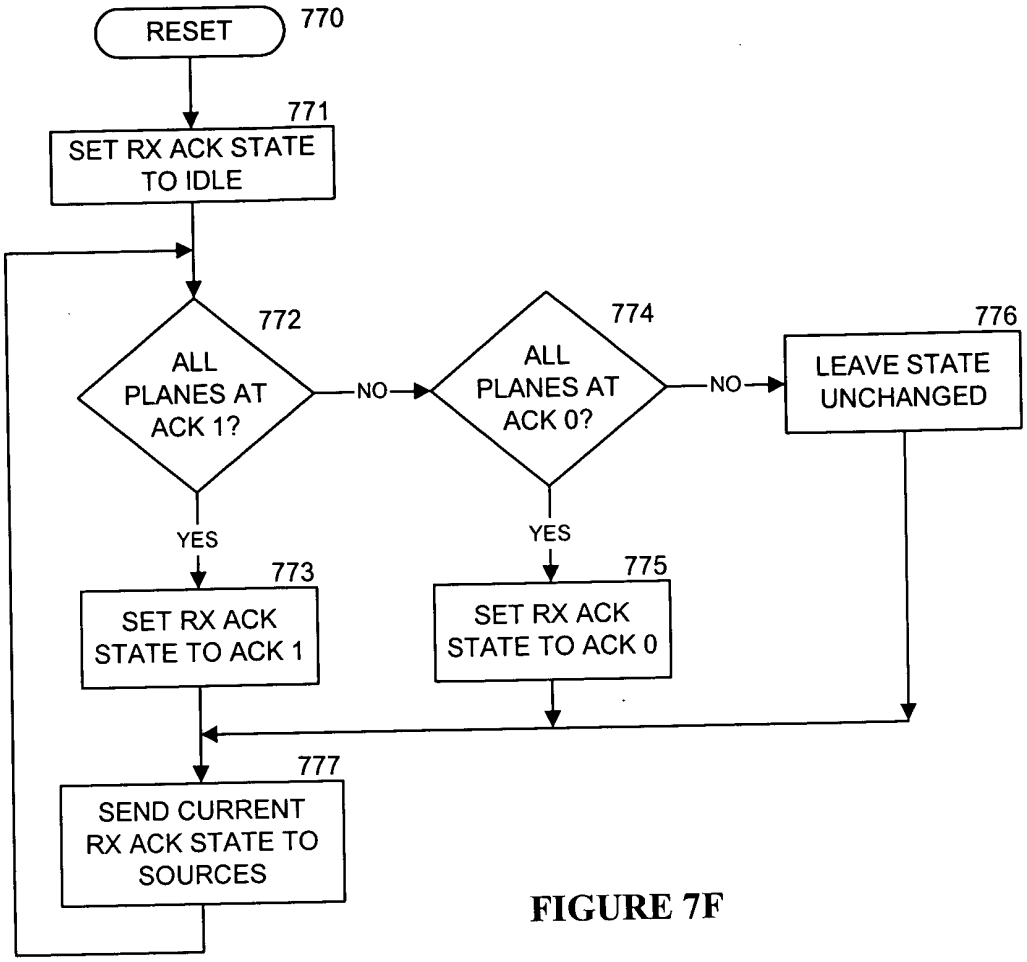
RESET
770
771
SET RX ACK STATE TO IDLE
772
ALL PLANES AT ACK 1?
NO
774
ALL PLANES AT ACK 0?
NO
776
LEAVE STATE UNCHANGED
YES
YES
773
SET RX ACK STATE TO ACK 1
775
SET RX ACK STATE TO ACK 0
777
SEND CURRENT RX ACK STATE TO SOURCES

FIGURE 7F

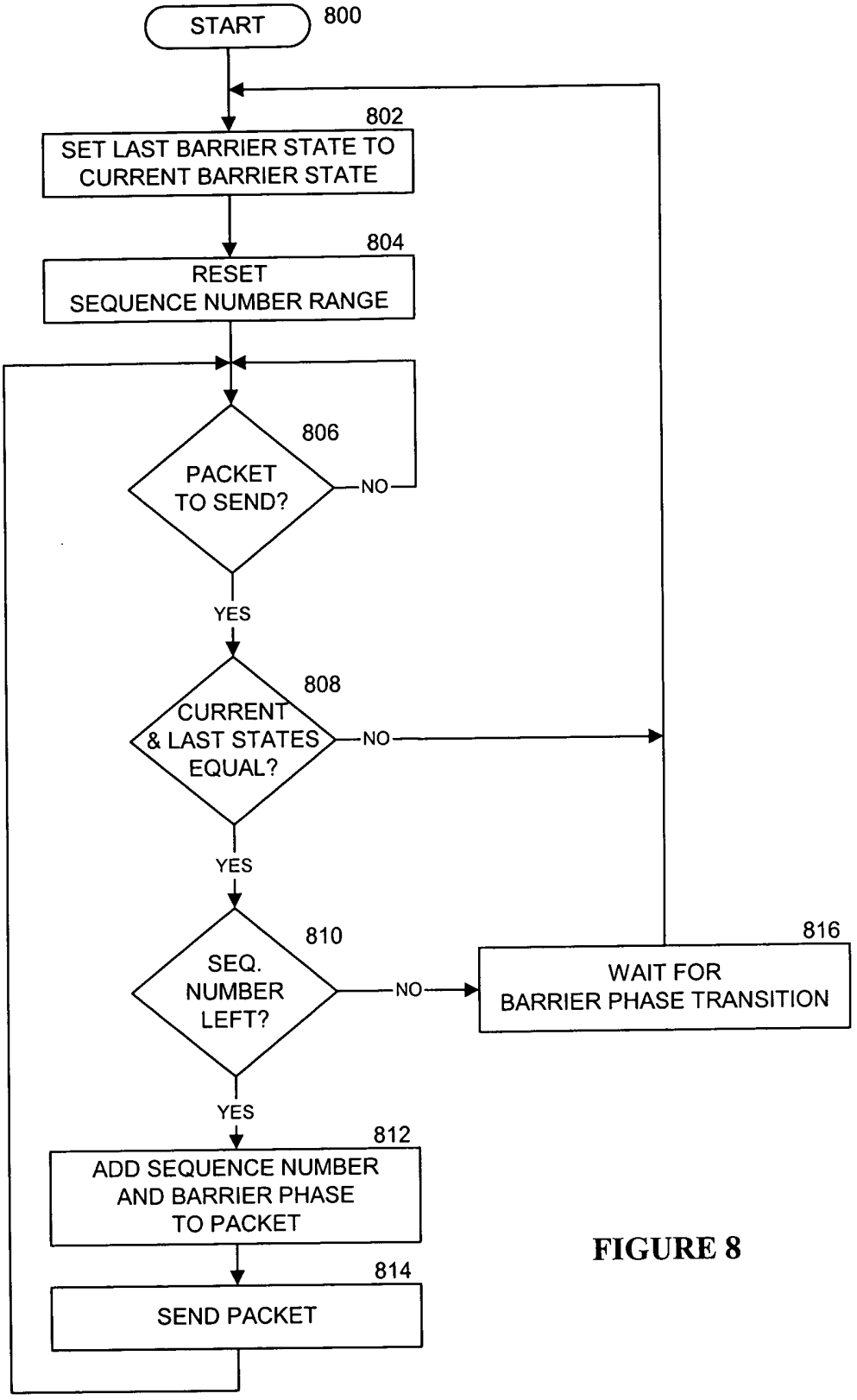
START
800
802
SET LAST BARRIER STATE TO CURRENT BARRIER STATE
804
RESET SEQUENCE NUMBER RANGE
806
PACKET TO SEND?
NO
YES
808
CURRENT & LAST STATES EQUAL?
NO
YES
810
SEQ. NUMBER LEFT?
NO
816
WAIT FOR BARRIER PHASE TRANSITION
YES
812
ADD SEQUENCE NUMBER AND BARRIER PHASE TO PACKET
814
SEND PACKET

FIGURE 8

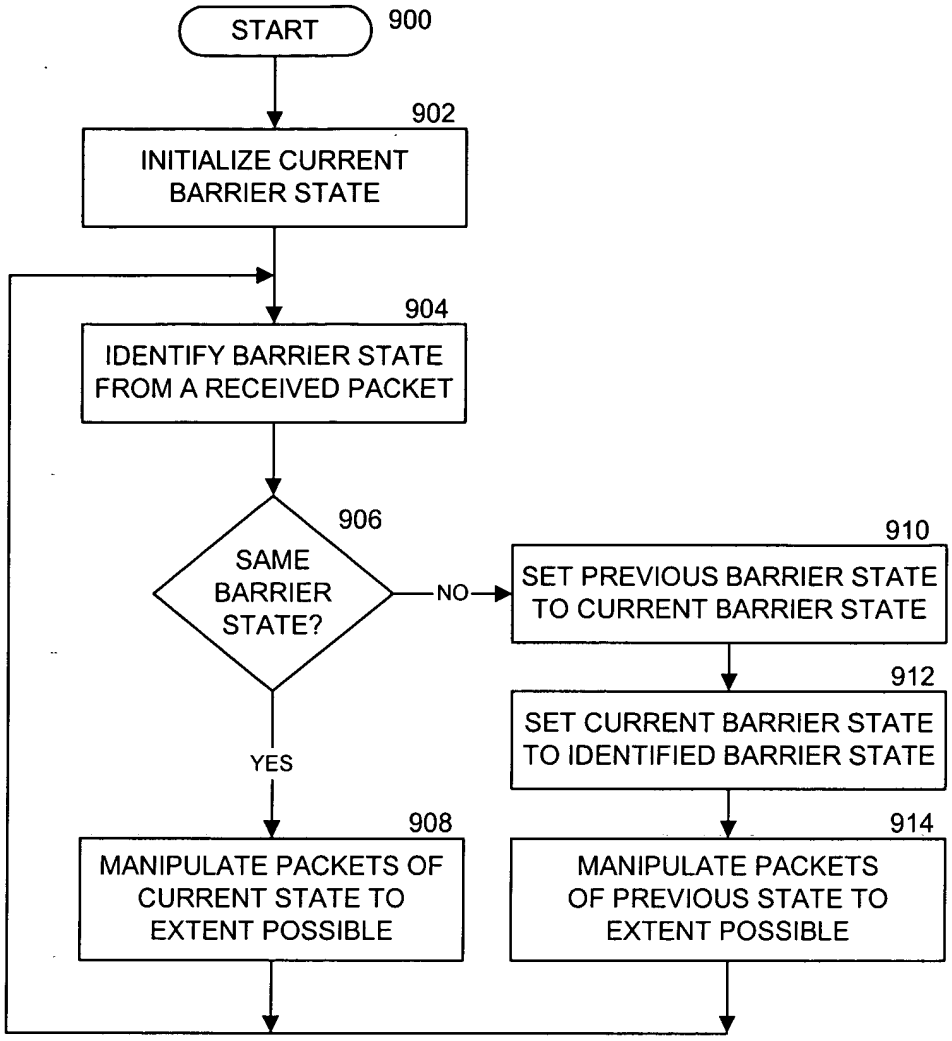
START
900
902
INITIALIZE CURRENT BARRIER STATE
904
IDENTIFY BARRIER STATE FROM A RECEIVED PACKET
906
SAME BARRIER STATE?
NO
910
SET PREVIOUS BARRIER STATE TO CURRENT BARRIER STATE
912
SET CURRENT BARRIER STATE TO IDENTIFIED BARRIER STATE
914
MANIPULATE PACKETS OF PREVIOUS STATE TO EXTENT POSSIBLE
YES
908
MANIPULATE PACKETS OF CURRENT STATE TO EXTENT POSSIBLE

FIGURE 9